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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,592	07/22/2003	Cheng-Hsien Chou	BHT-3226-39	5852
7590 05/01/2008 TROXELL, LAW OFFICE PLLC SUITE 1404 5205 LEESBURG PIKE FALLS CHURCH, VA 22041			EXAMINER CHANG, RICK KILTAE	
			ART UNIT 3726	PAPER NUMBER
			MAIL DATE 05/01/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/623,592

**Applicant(s)**

CHOU ET AL.

**Examiner**

Rick K. Chang

**Art Unit**

3726

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 February 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 14-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
- 3) ☐ Information Disclosure Statement(s) (PTO/SE/US)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(c), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(c) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/21/08 has been entered.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

There are numerous phrases and clauses in the claims that are vague, indefinite, and/or awkwardly and confusingly worded, and therefore, are not fully understood. The following are examples:

Claim 14, line 6: it is unclear whether the two copper clad layers are on the core or part of the core.

Claim 14, lines 9-11: “forming” and “lamination” are two separate process. It is unclear whether “a dielectric layer” is formed into a laminated dielectric layer or laminated to form a laminated dielectric layer.

Claim 14, lines 12-13: “a circuit” and “two circuit layers” constitute different number of circuits. It is unclear how “a circuit” can form “two circuit layers.”

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 14-15 and 17, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al (US 4,882,454) in view of Kiyota et al (US 5,263,248), and further in view of Haba et al (US 6,675,469), Cutting et al (US 5,638,597) and Shin et al (US 6,405,431).

Re claims 14, 17: Peterson discloses preparing a core (102) including a thin compound plate having an inner layer made of a material and two copper layers (105) provided on two outer sides of the inner layer;

performing a circuit (301,302) formation on the two copper layers of the core by way of etching to form two circuit layers on the two outer sides of the inner layer (col. 3, lines 20-21), respectively;

forming a laminated dielectric layer (101) from the prepreg material and a copper layer are sequentially formed on each of the two circuit layer by way of lamination (105), so that a four-layer PCB is formed (see Fig. 1);

forming a circuit on the copper layers to form another two circuit layers on outer sides of the two dielectric layers (105 are circuits);

forming two resin layers (101; epoxy is a resin material) being by way of applying a dielectric material (101) on outer sides of the two circuit layers (105);

forming necessary conductive holes on the resin layers (where 314s are located) by performing laser drilling and mechanical drilling (col. 3, lines 37-38 and lines 46-50), respectively, to form a PCB (Fig. 5);

plating the PCB with copper to form a copper-plating layer on all outer surfaces of the PCB (col. 3, lines 49-54);

performing the circuit formation by way of etching the copper-plating layer to form two additional circuit layers (col. 3, lines 49-54); and

forming another two laminating dielectric layers (101), and another two copper clad layers being sequentially formed on outer sides of the two additional circuit layers (105) by way of lamination to form the 8-layer PCB (the claim does not limit the prior art form having more than 8-layers).

Peterson fails to disclose a prepreg material and two copper clad layers; forming a resin build-up process through liquid epoxy coating or dry film type epoxy laminating on the two circuit layers.

Haba forming a resin build-up process through epoxy laminating on the two circuit layers (20).

Kiyota discloses a prepreg material is a resin-impregnated fiberglass fabric (col. 3, line 53).

Shin discloses two copper clad layers (10).

Cutting discloses dry film type epoxy (col. 3, line 56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peterson by a prepreg material and two copper clad layers; forming a resin build-up process through liquid epoxy coating or dry film type epoxy laminating on the two circuit layers to the Peterson's PCB, as taught by Haba, Kiyota, Shin and Cutting, for the purpose of utilizing proven materials that are well known in the PCB manufacturing industry to save manufacturing cost and research and development time.

Re claim 15: Peterson discloses etching the conductive layers to form circuits (col. 3, lines 44-54), except for copper clad layers.

Shin discloses two copper clad layers (10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peterson by copper clad layers to the Peterson's PCB, as taught by Shin, for the purpose of utilizing proven materials that are well known in the PCB manufacturing industry to save manufacturing cost and research and development time.

7. Claim 16, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al (US 4,882,454)/Kiyota et al (US 5,263,248)/Haba et al (US

6,675,469)/Cutting et al (US 5,638,597)/Shin et al (US 6,405,431) as applied to claims 14-15 above, and further in view of Fujii et al (US 6,591,491).

Peterson/Kiyota/Haba/Cutting/Shin fail to disclose plating gold to form two other circuit layers.

Fujii discloses plating gold to form two other circuit layers (32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Peterson/Kiyota/Haba/Cutting/Shin by plating gold to form two other circuit layers to the Peterson/ Kiyota/Haba/Cutting/Shin's PCB, as taught by Fujii, for the purpose of utilizing proven materials that are well known in the PCB manufacturing industry to save manufacturing cost and research and development time as well as providing the one of the best electrically conductive material known to mankind.

### ***Response to Arguments***

8. Applicant's arguments filed 2/21/08 have been fully considered but they are not persuasive.

The claims do not limit the prior art from having more than 8 layers.

The term "lamination" is broadly interpreted, since the claim does not further limit how, what form or what state the layers are laminated. The examiner maintains that Peterson discloses laminating.

### ***Conclusion***

9. Please provide reference numerals (either in parentheses next to the claimed limitation or in a table format with one column listing the claimed limitation and another column listing corresponding reference numerals in the remark section of the response to the Office Action) to

all the claimed limitations as well as support in the disclosure for better clarity (optional).

Applicants are duly reminded that a full and proper response to this Office Action that includes any amendment to the claims and specification of the application as originally filed requires that the applicant point out the support for any amendment made to the disclosure, including the claims. See 37 CFR 1.111 and MPEP 2163.06.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rick K. Chang whose telephone number is (571) 272-4564. The examiner can normally be reached on 5:30 AM to 1:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Bryant can be reached on (571) 272-4526. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rick K. Chang/



Art Unit: 3726

Primary Examiner, A.U. 3726

RC

May 6, 2008